TRANSISTORS and TRANSISTOR AMPLIFIERS

I. PURPOSE
To familiarize with the characteristics of transistors, how to properly implement its DC bias, and illustrate its application as small signal amplifiers. The bipolar junction transistor as well as the field effect transistor will be considered.

II. THEORETICAL CONSIDERATIONS

II.1 Bipolar Junction Transistor

II.2 Field Effect Transistor (FET)

II.1 Bipolar Junction Transistor

Transistor modeled as a current amplifier
Transistor is a 3-terminal device: emitter, base, collector. They are available in two flavors: npn and pnp.

Diode model: An initial understanding of the transistor can be obtained considering the base-emitter and the base-collector as diodes.

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In that context, let’s analyze in more detail the npn transistor.

- Consider first the emitter-base diode.
Fig. 1 Analysis of the base-emitter pn junction. **Left:** Energy band diagram of the (base-emitter) pn junction under equilibrium; a barrier exist for the electrons to cross from the n-region to the p-region. The red line is the Fermi level. Under external forward bias (voltage at \( p \) greater than the voltage at \( n \)), the barrier is lowered and a forward bias flow of electrons is established. **Center:** The forward bias current depends critically on the base-emitter voltage. The current is significant when the \( V_{BE} \) voltage is greater than a threshold voltage (~ 0.7 volt for the case of silicon). **Right:** When the \( p \)-base is lightly doped the net bias current is mainly constituted by electrons from the n-doped emitter.

The p region is made lightly doped, thus the forward current is constituted mainly by electrons from the n-doped emitter.

The arriving electrons implicitly become **minority carriers** in the host p-region; subsequently they move to the collector by diffusion. (The finite time taken by the minority carriers to cross the base limits the high-frequency response of the transistor.)

The p region (base) is made narrow (~ 0.5 \( \mu \)m) compared to the diffusion length. That way, out of a number of arriving electrons only a few are lost by recombination with the host holes at the base and most diffuse to the depletion region of the base collector junction (see Fig.3).

- **The base-collector diode.**

  Since \( |V_2| > |V_1| \), the latter being of the order of 0.7 V, this diode is **reversed biased**. Thus, the role of the \( V_{BC} \) voltage is just to sweep the charges that, after arriving from the emitter to the base, diffuse to the collector.

  For this reason, it is found that the collector current varies very little with the collector voltage.

**Fig. 2 Transistor currents Left:** Injection of majority carriers from the emitter. A relatively small numbers reaches the base but most are swept towards the collector. **Right:** Equivalent picture of the left diagram, but in terms of the more formal currents.
Fig. 3 Transistor circuit configuration with the npn and depletion layer regions. The injection of electron from the emitter to the base is controlled by the $V_{EB}$ voltage. By making the width of the base $W_B$ very thin (smaller than the diffusion length), the electrons diffuse towards the BC junction. In the BC depletion region the electron are swept by the reversed bias. Notice, the collector current will be practically independent of the $V_{BC}$ voltage, since any value of the reverse volatage would be enough to sweep the electrons (that is, the collector current will change little when changing the load resistor $R_L$).

When the transistor is properly electrically biased, the net result is:

$I_C$ is roughly proportional to $I_B$

$$I_C = \beta I_B$$  \hspace{1cm} (1)

The so called current gain $\beta$ is typically about 100.

($\beta$ is not a good transistor parameter; its value can vary from 50 to 250. It also depends on the collector current, collector-to-emitter voltage, and temperature.)

This represents the usefulness of the transistor. A small current into the base controls a much larger current flowing into the collector. That is, the transistor is a current amplifier.

II.2 Field Effect Transistor (FET)

A field effect transistor is a three-terminal device in which the current through two terminals is controlled at the third (similar to the bipolar junction transistor.)

Field effect devices are controlled by a voltage at the third gate terminal (rather than by a current like in the BJT.) The FET nonexistent gate current is its most important characteristics. The resulting high input impedance (which can be greater than $10^{14}$ $\Omega$ is essential in many applications.

FET is a unipolar device; that is, the current involves only majority carriers.

The field effect transistors come in different forms:

- Junction FET (JFET) based on controlling the depletion width of reversed-biased p-n junctions.
- Metal-semiconductor FET (MESFET) results when the p-n junction is replaced by a Schottky barrier (i.e. a metal-semiconductor junction.)
- When the metal is separated from the semiconductor by an insulator, a MISFET results. When an oxide layer is used as the insulator the device is called a MOSFET.

The various types of FET are characterized by **high input impedance**, since the control voltage is applied to a reversed-biased junction, or Schottky barrier, or across an insulator.

FETs are well suited for controlling the switch between a conducting state and a nonconducting state. That is, they fit very well in digital circuits. In fact MOS transistors are used in semiconductor memory devices.

**II.2.1 Junction Field Effect Transistor**

A $n$-channel JFET has three terminals: gain (G), drain (D) and source (S).

The input signal is the voltage applied between the gate and source.

The output signal is the current from drain to source ($e^-$ from source to drain.)

![Diagram of a JFET](image)

**Fig. 3 Left:** Terminals in a FET. **Right:** For proper operation the (gate-channel) pn junction must be reversed biased, so that a depletion region is formed as shown. The drain is operated at a positive voltage relative to the source, hence the gate-drain end is more strongly reversed biased (thicker depletion layer and thinner channel) than the gate-source end (thinner depletion layer and thicker channel.) The depletion region acts as a non-conductor; the remainder of the channel acts as a resistor with peculiar properties.

**Input characteristics.**

Because the gate-channel pn junction is reversed biased, very little current flows into the gate. Consequently, the input impedance of the device is extremely high, up to $10^{12}\Omega$, and very little energy is required to control the device.

The **gate controls the current in the channel** through an electric field that affects the depletion region.
Output characteristics.
Let’s analyze the circuit for a given fixed value of the input voltage $V_{GS}$ (gate-source voltage.)

- Let choose $V_{GS} = 0$ V:
  
  For increasing, but small, values of the drain-source voltage $V_{DS}$, the current increases, similar to the case of a simple resistor (ohmic region.)

  As $V_{DS}$ increases further, the current begins to level off because the channel narrows at the drain end (see Fig.3.) When the drain-source voltage reaches the value $V_{DS} = -V_{P}$ ($V_{P}$ is called the pinchoff voltage) a region of the conducting channel reaches a minimum size at the drain end.

  The current remains constant upon further increases of the $V_{DS}$. This is the saturation region. (The electrons in the channel are free to move out of the channel and then through the depletion region attracted by the $V_{DS}$ voltage. The depletion region is free of carriers and has a resistance similar to silicon. However, an increase of $V_{DS}$ (which would tend to increase the channel current) will also increase the distance from drain to the pinch-off point thus increasing the channel resistance. As a result, these two trends compensate as to keep the channel current constant.)

In the saturation region (although it would be better to call it the “active region”) the drain current is controlled totally by the input signal.

![Fig. 4 Output characteristics of a JFET. A pinch-off voltage equal to -4 volts has been assumed. The arrow in the JFET symbol is to identify the source (S) (because, otherwise, the source and the drain are architecturally symmetric).](image)

- For lower (negative) values of $V_{GS}$, the voltage $V_{DS}$ at which pinchoff occurs decreases. The maximum current also decreases.

- For $V_{GS} < V_{P}$:
  
  The FET is cut off; no current flows regardless of $V_{DS}$. The blockage of current occurs for the same reason (the growth of the depletion region due to the reversed bias).
III. EXPERIMENTAL CONSIDERATIONS

III.1 The Bipolar Junction Transistor

III.1.1 Transistor’s characteristic curves. Current gain $\alpha$ and the $\beta$ value

III.1.2 DC bias circuit and the operating point

III.1.3 Small signal amplifier (not required in Winter 2013)

III.2 The Field Effect Transistor

III.2A The Junction Field Effect Transistor (JFET)

III.2B The Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

III.1.1 Transistor’s characteristic curves. Current gain $\alpha$ and the $\beta$ value

We will use general purpose transistors: 2N 2222, 2N 3906, or the npn 2N 3904. Use a npn transistor and setup the circuit indicated in the figure below.

Select $R_B$ and $R_C$ such that $I_C$ fall in the range of mA, and $I_B$ in the order of 5 $\mu$A to 200 $\mu$A. The suggested use of variable resistors is for you to be able to do the proper changes as to keep the $I_B$ constant while obtaining the trace of one of the current collector curves.

**TASK:** Obtain the characteristic curves of the transistor. Plot about 04 curves, corresponding to different values of base current

Fig. 5 Source: http://www.physics.csbsju.edu/trace/nFET.CC.html
**TASK:** Estimate the experimental value of the transistor current gain

\[ \alpha = \frac{i_C}{i_E}. \]  

(2)

Keep in mind that usually the current gain is described in terms of the \( \beta \) value of the transistor, the latter being defined as,

\[ \beta = \frac{i_C}{i_B} = \frac{i_C}{i_E - i_C} = \frac{\alpha}{1 - \alpha} \]  

(3)

**III.1. 2  DC bias circuit and the operating point**

Given the transistor curves characteristics, our objective is to bias the transistor properly as to make it function around a given operating point inside the active region (point P in the diagram below, for example.) The procedure will help us understand **how the output voltage depends on the input voltage.**

**Fig. 5** Grounded-emitter setup for obtaining the collector current characteristics. \( I_B \) is approximately constant across the active region.

**Fig. 6** Given the collector current characteristics. \( R_C \) and \( R_B \) should be selected to have the transistor operating around the point P in the active region.
How to choose \( R_C \)?

Load line analysis

Even though we do not know \( I_C \) neither \( V_{CE} \), a relationship between them can be obtained through the Kirchhoff’s law applied to the right side branch of the circuit above (and reproduced below for convenience.);

\[
15V - I_C \cdot R_C - V_{CE} = 0,
\]

which leads to,

\[
I_C = \frac{15V}{R_C} - \frac{1}{R_C} V_{CE} \quad (I_C)
\]

decreases linearly with \( V_{CE} \).)

If we want to work with, for example, a current base of 50 mA, many values of \( R_C \) are possible. Still, there is a restriction to be satisfied, which is not to exceed the transistor’s heat dissipation tolerance. For example, the data sheet may specify,

\[
V_{CE,\text{max}} \cdot I_{CE,\text{max}} < 350 \text{ mWatts}
\]

Applying this condition to our case, one obtains

\[
(15 \text{ V}) \cdot \left( 15 \text{ V}/R_C \right) < 350 \text{ mWatts}
\]

Thus, in this case, a resistor \( R_C > 1 \text{ K\Omega} \) would be good enough

How to choose \( R_B \)?

Since we want to operate the transistor at the point \( P \), that is a current base of 50 \( \mu \text{A} \), all we have to do is to choose an \( R_B \) that allows delivering a current of that magnitude

\[
R_B \sim \frac{15V - 0.7V}{50 \mu \text{A}}
\]

which takes into account that, when operating in the active region, the base voltage is about 0.7
V (for silicon transistors.)
The operating point \( P \) results then from the intersection of the load line and the transistor curve corresponding to 50 \( \mu A \).

**TASK:** Set up the transistor to work in one point of the active region

**How the output voltage depends on the input voltage**

Instead of using a fixed \( V_{in} \) voltage, vary its value a bit as to produce slightly different base currents. The diagram below helps illustrate the expected variation of the \( V_{CE} \) voltage.

![Diagram showing how the output voltage depends on the input voltage](image)

Fig. 9 Small variations of \( I_B \) moves the operating point \( P \) along the load line, causing a variation of \( V_{CE} \) (and, correspondingly, a variation in \( I_C \)).

**TASKS:**

Make a plot of \( V_{out} \) vs \( V_{in} \) (Notice, in this case, \( V_{out} = V_{CE} \))

Verify that the plot looks like the graph shown in the figure at the right.

From this experimentally obtained graph, evaluate the voltage gain: \( \Delta V_{out} / \Delta V_{in} \)

![Diagram showing the greater \( V_{in} \), the greater \( I_B \), the greater \( I_C \) and greater drop of voltage across \( R_C \), the lower \( V_{CE} \) voltage.](image)

Fig. 10 The greater \( V_{in} \), the greater \( I_B \), the greater \( I_C \) and greater drop of voltage across \( R_C \), the lower \( V_{CE} \) (output voltage.) Thus, small variations of the input voltage around a given value will be 180° out of phase with the output voltage.

NOTE: Notice from figures 9 and 10, that the greater \( V_{in} \), the greater \( I_B \), the greater \( I_C \) and greater drop of voltage across \( R_C \), the lower \( V_{CE} \) (output voltage.) Thus, small variations of the input voltage around a given value will be 180° out of phase with the output voltage.
III.1.3 Small signal amplifier (Not required in 2013) Jump to section III.2

A large signal amplifier operates the transistor in its full range of operation, from near cutoff to near saturation (from small IC currents to large currents). Such an operation mode is quite suitable for digital electronics application, where LOW and HIGH signal levels determine the “0” and “1” binary information.

Other applications require small-signal amplifiers. For a given configuration, where the transistor operates at a given point of the active region, a small modulation of the base-current translate into a modulation of the collector current (picture a small audio signal being amplified by the transistor). If high amplifications are required, several small-signal amplifiers can be cascaded in series. In this laboratory session we will construct and analyze just one small-signal amplifier stage.

A small-signal amplifiers must have:

- a dc bias circuit for placing the transistor in its amplifying region (VERY IMPORTANT).
- a mean for introducing the input signal
- a mean for supplying its output signal to the next stage.

The circuits used in the previous section deal with the first two aspects. But, as it turns out, such circuits are very sensitive to temperature variation. For that reason, we will be modify it a bit, but their equivalence with our older circuit will become transparent in the course of the discussion. Once the circuit is properly DC biased, we will proceed to input a small AC signal. (The coupling of a circuit stage to another will be addressed in Lab #4, when we study the concept of input and output impedance).

III.1.3.A Modified DC-bias Circuit. Placing the transistor in its amplifying region.

The simple bias circuit in Fig. 9 above is generally not satisfactory because the operating point shifts drastically with temperature.

A more satisfactory transistor bias is obtained when using a voltage divider, as shown in Fig. 11.

- **TASK:** Construct the circuit shown in Fig. 11.

**Thevenin equivalent circuit analysis**

We can use the Thevenin’s theorem to show the equivalence between the circuits in Fig. 9 and Fig. 11. This is made more evident by re-drawing Fig. 11 as shown in Fig. 12 below.

Through the Thevenin theorem one can claim that both circuits, the ones at the left and right sides of Fig.12 are equivalent. Analyzing the shaded area one obtains:

- The Thevenin voltage \( V_{BB} \) is the open-circuit voltage (voltage across XY in the circuit...
when no external load is applied \( V_{BB} = \frac{V_{CC}}{R_1 + R_2} R_1 \). \((V_{BB} = (10V/55.6k\Omega)(5.6k\Omega) = 1V.\)

- \( R_B \) designates the Thevenin equivalent series resistance. The short circuit currents (i.e. the currents when X and Y are shorted) are \( V_{CC}/R_2 \) and \( V_{BB}/R_B \) respectively. Since the circuits are equivalent these two current must be equal. Hence, \( R_B = \frac{R_2 R_1}{R_1 + R_2} \); using the value for \( V_{BB} \) obtained above, results \( R_B = \frac{R_2 R_1}{R_1 + R_2} \) \((R_B = (50k \Omega \times 5.6k \Omega) / (55.6k \Omega) = 5k \Omega \).

Fig. 12 DC bias circuit and its Thevenin equivalent. The latter helps to calculate the different parameters associated to the intended operating point of the transistor (using the analysis described in the previous section) based on the values of \( R_1 \) and \( R_2 \).

- **TASKS:** For the final values that you use for \( R_1 \) and \( R_2 \) calculate the Thevening values for \( V_{BB} \) and \( R_B \).

Select the proper value of \( R_C \) such that the transistor work in the active region.

**THIS IS VERY IMPORTANT.** More specifically, choose \( R_C \) such that \( V_{CE} \) is ~ 4 Volts. \((\text{An } R_C \sim 1 \text{ k}\Omega \text{ should work}).

Fig. 13 Equivalent representation of the circuits in Fig. 12.

**III.1.3.B Connecting to an oscillator**

Once the transistor is properly DC biased \((V_{CE} \sim 4 \text{ volts})\), proceed to connect the voltage from a signal generator. See Figure 14. If the oscillator is connected directly at the \( V_{in} \), unwanted
DC voltage offset from the oscillator may change the bias level and/or draw some current away from $I_b$, and thus potentially spoil the operation point designed in the previous section. As a precaution, it is normally convenient to put a capacitor in series with the oscillator to block the flow of DC current. (You could try $C_1 = 1 \mu F$ but be aware of the frequency range of operation. Since the impedance of the capacitor is frequency dependent, make sure the capacitive reactance is small with respect to the other resistance you use at the input; i.e. you need a resistance to limit the base current).

**TASK:**
Couple a small sinusoidal signal (start using ~0.03 V amplitude) into the circuit shown in Fig. 14 (Left diagram).
Monitor the input and output signals in the oscilloscope.

It is convenient to first monitor the output voltage $v_{out}$ with the oscilloscope set to DC mode, so you can track whether its value is saturate or not.

Measure the AC voltage amplification, as well as the relative phase between the input and output voltage. (For this measurement, you may want to switch monitoring the output voltage with the oscilloscope in ac-mode).

For the coupling capacitance $C_1$ that you choose ($C_1 = 1 \mu F$ for example) find out the range of frequencies for which the circuit works properly. Find out also the range of input-voltages amplitude tolerated by the circuit.

Make the circuit to work in the low frequency (tens of hertz) and high frequency range (tens of kHz or higher). You may need a different capacitor for each of these two cases.

**Notice:**
Your circuit may not allow putting an ac-signal input signal $V_{in}$ of amplitude greater than ~0.3 V (actually the exact value depends on the value you select for $R_s$), otherwise you would drive the transistor out of its operation range (this will be reflected in the clipping of the output signal).

Try $R_s = 1 \Omega$ or 10 kΩ

**Fig. 14 Left:** Small signal amplifier circuit. **Right:** Equivalent circuit, which helps to differentiate the additional (AC) base current injected by the signal generator from the DC base current established by the bias circuit.
Evaluate the maximum amplitude of the input ac-signal that your circuit tolerates (i.e. avoiding clipping in the output signal). Check whether a Rs= 1 kΩ or Rs= 10 kΩ works better in this regard.

Monitor the voltage \( V_B \) at the base of the transistor all the time (with a multi-meter or, better, with the oscilloscope); the value should be \( \sim 0.7 \) volts. Whenever you observe the output signal “clipping” it may be because \( V_B \) is deviating very much from this value (If \( V_B \) is too high the transistor lead to saturation; if \( V_B \) is too low the transistor is off).

Eventually, you may need to change the value of RC to have the voltage \( v_{out} \) in the proper range (i.e. \( v_{out} \) has to be greater than 0.7 volt, so it can allow ac variation without turning off the transistor.)

It is convenient to first monitor the output voltage \( v_{out} \) without the capacitor, so it can be tracked whether its value is saturate or not. For that purpose monitor \( v_{out} \) with the oscilloscope set to DC mode. After you find your circuit working properly, insert the capacitor \( C_2 \) (Fig. 15).

![Circuit diagram](image)

**Fig. 15** Circuit is exactly the same in Fig. 14, except using an out coupling capacitor.

### III.2A The Junction Field Effect Transistor JFET

We will use the general purpose JFET 2N5457

**TASK:** Implement the JFET in the circuit outlined in Fig.4. Determine the characteristics curves, as well as the pinchoff voltage \( V_P \).

### III.2B The Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

**REFERENCES**


Even though the conductive channel formed by gate-to-source voltage no longer connects source to drain during saturation mode, carriers are not blocked from flowing. Considering again an n-channel device, a depletion region exists in the p-type body, surrounding the conductive channel and drain and source regions. The electrons which comprise the channel are free to move out of the channel through the depletion region if attracted to the drain by drain-to-source voltage. The depletion region is free of carriers and has a resistance similar to silicon. Any increase of the drain-to-source voltage will increase the distance from drain to the pinch-off point, increasing resistance due to the depletion region proportionally to the applied drain-to-source voltage. This proportional change causes the drain-to-source current to remain relatively fixed independent of changes to the drain-to-source voltage and quite unlike the linear mode operation. Thus in saturation mode, the FET behaves as a constant-current source rather than as a resistor and can be used most effectively as a voltage amplifier. In this case, the gate-to-source voltage determines the level of constant current through the channel.”